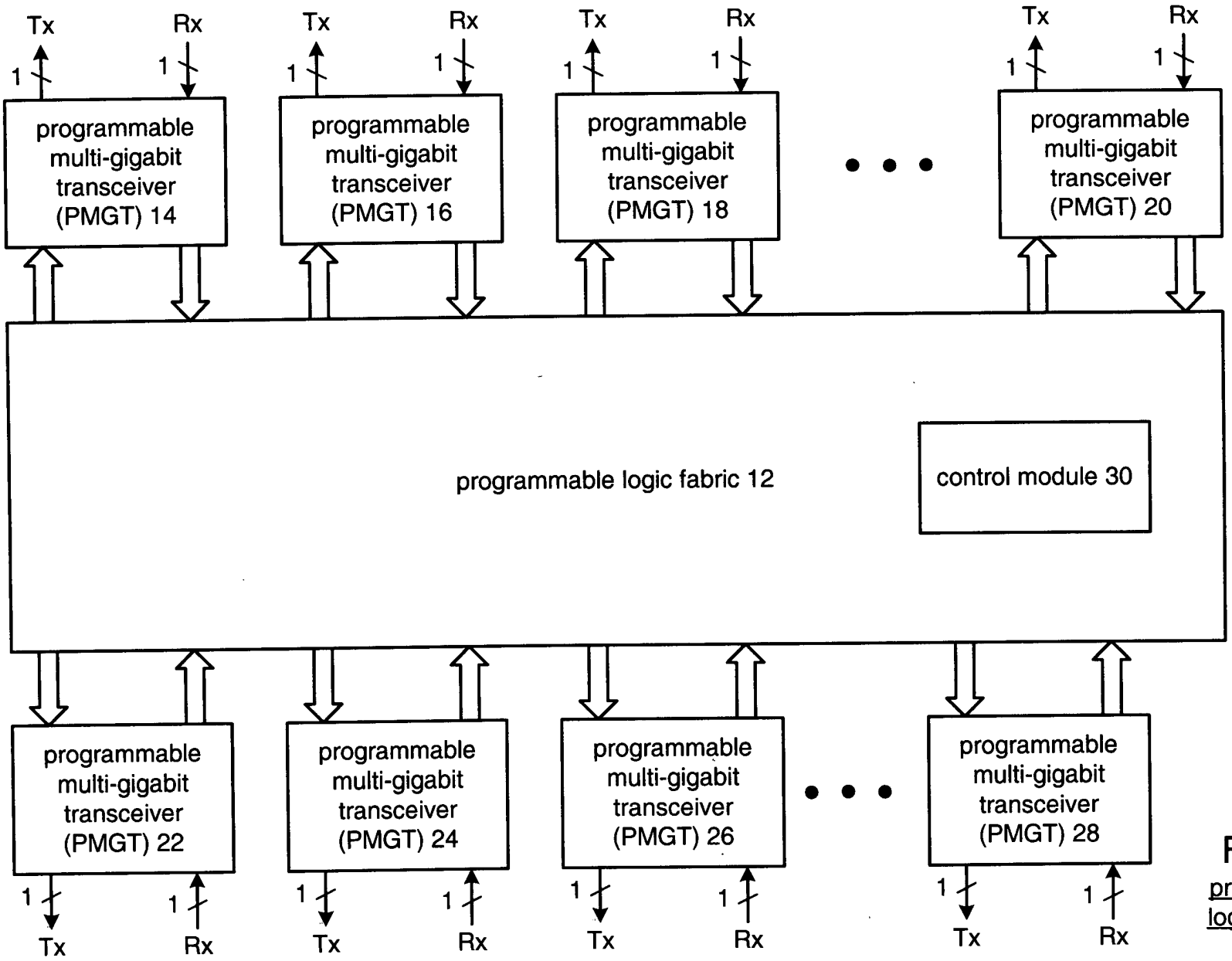

Figure 1
programmable logic device 10

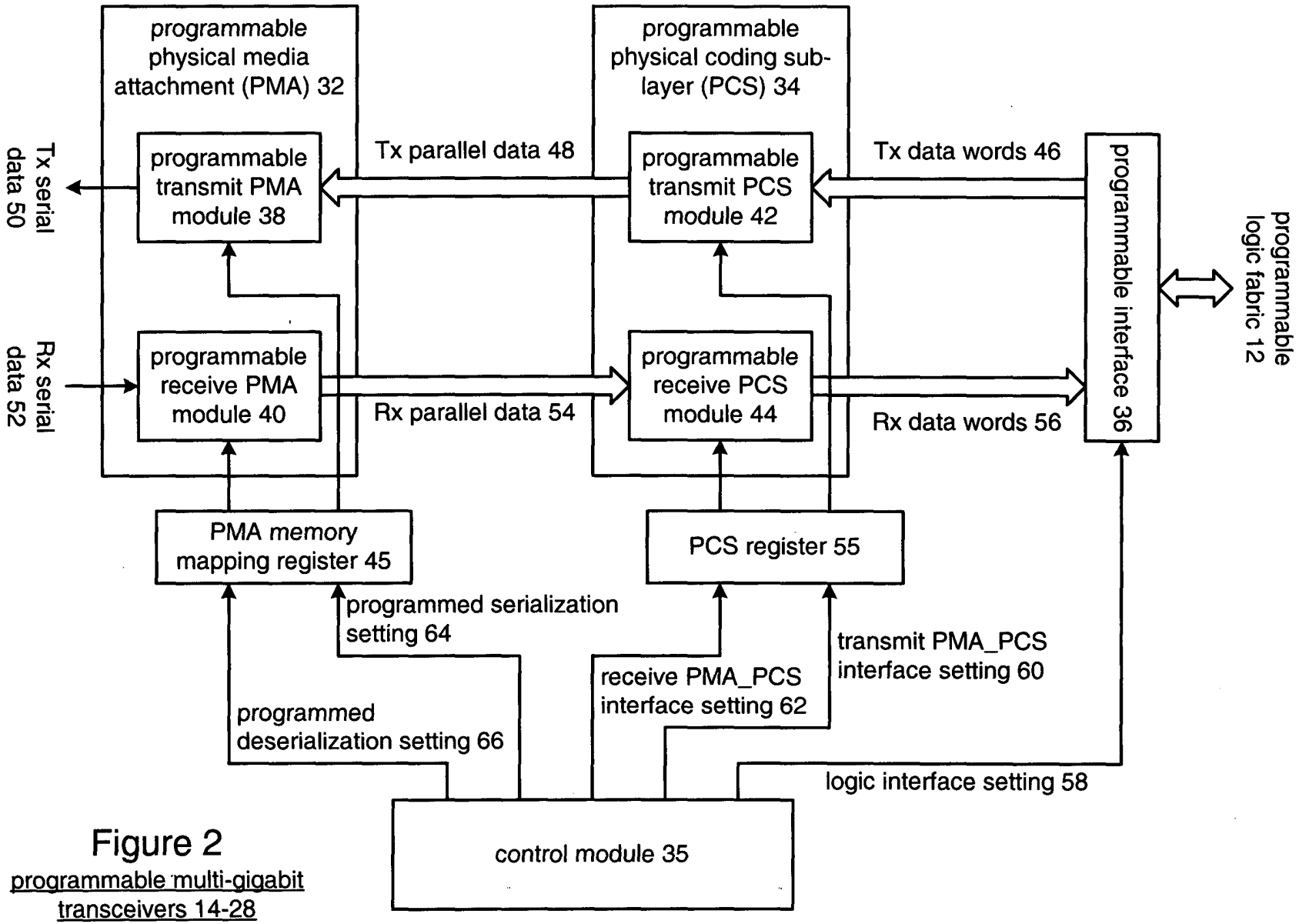

Figure 2
programmable multi-gigabit transceivers 14-28

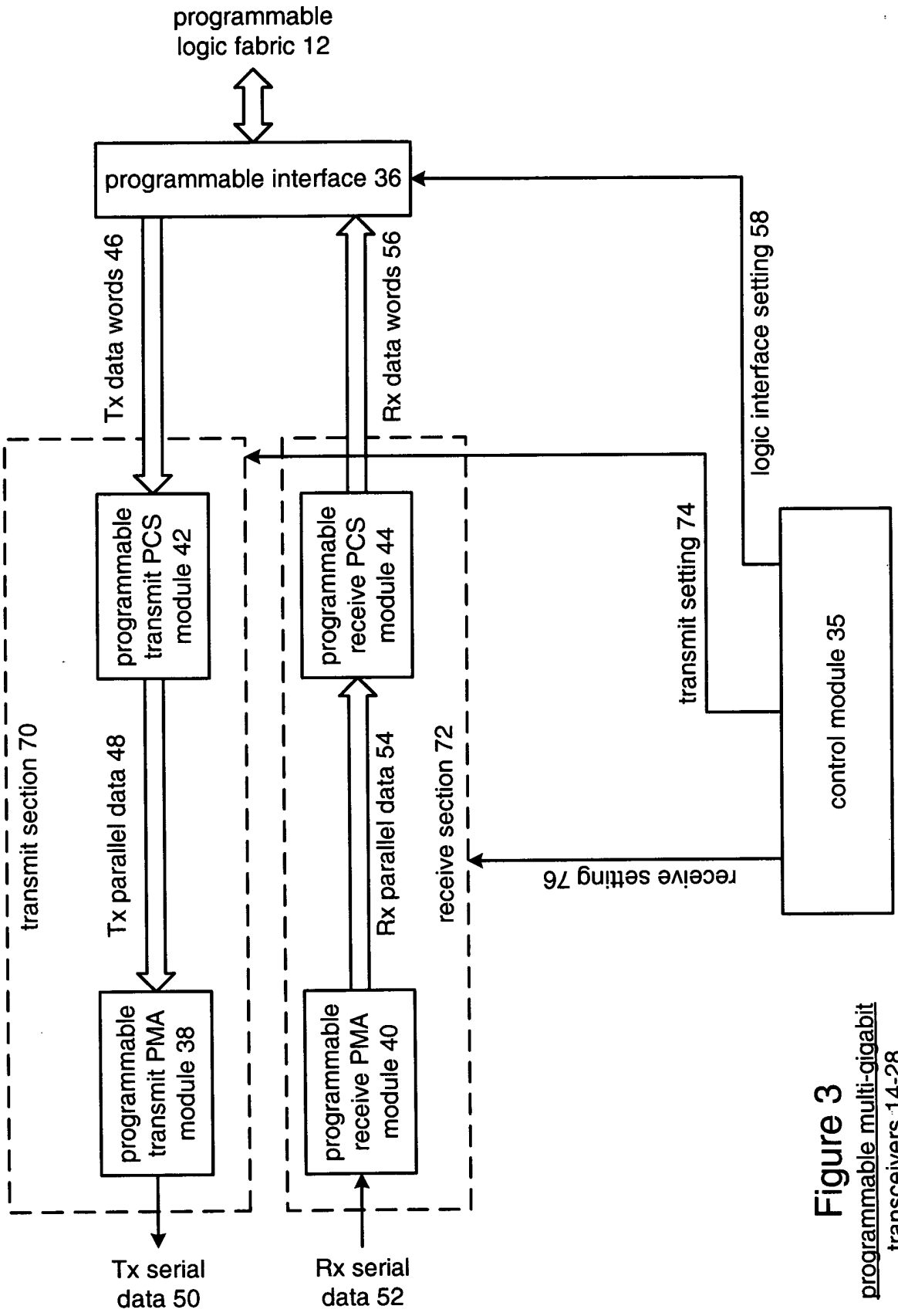

Figure 3
programmable multi-gigabit transceivers 14-28

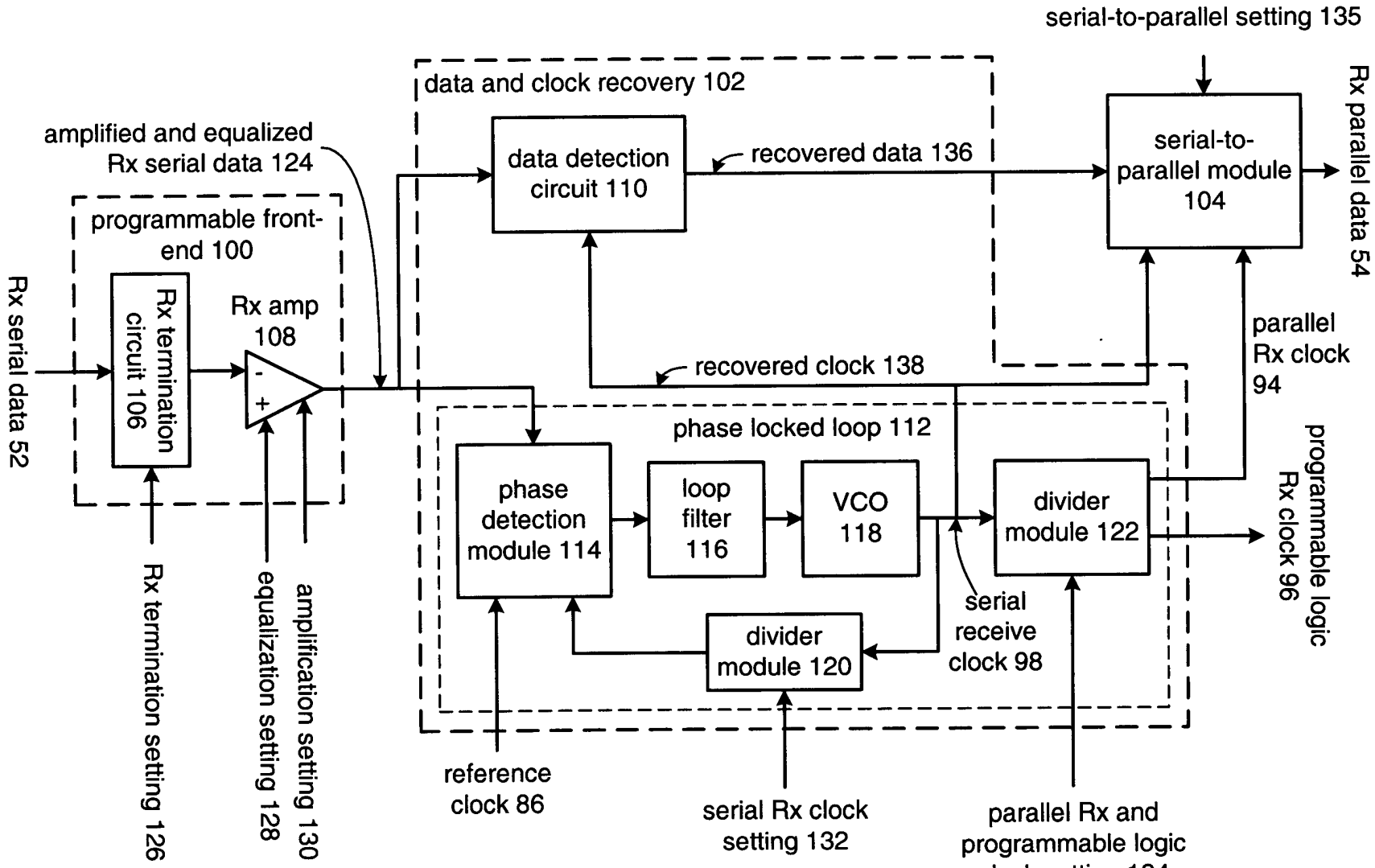

Figure 4A

programmable receive PMA module 40

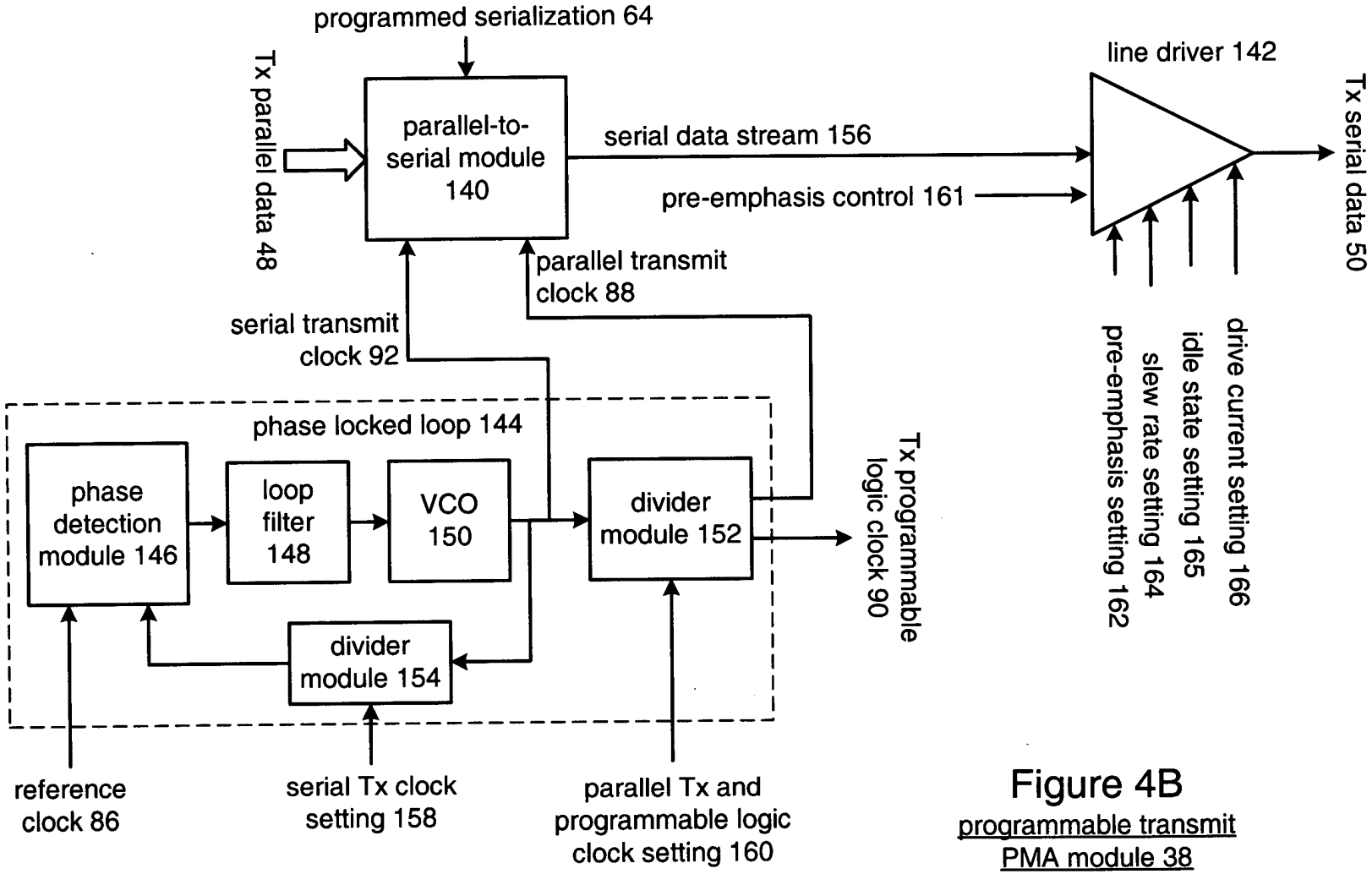

Figure 4B
programmable transmit PMA module 38

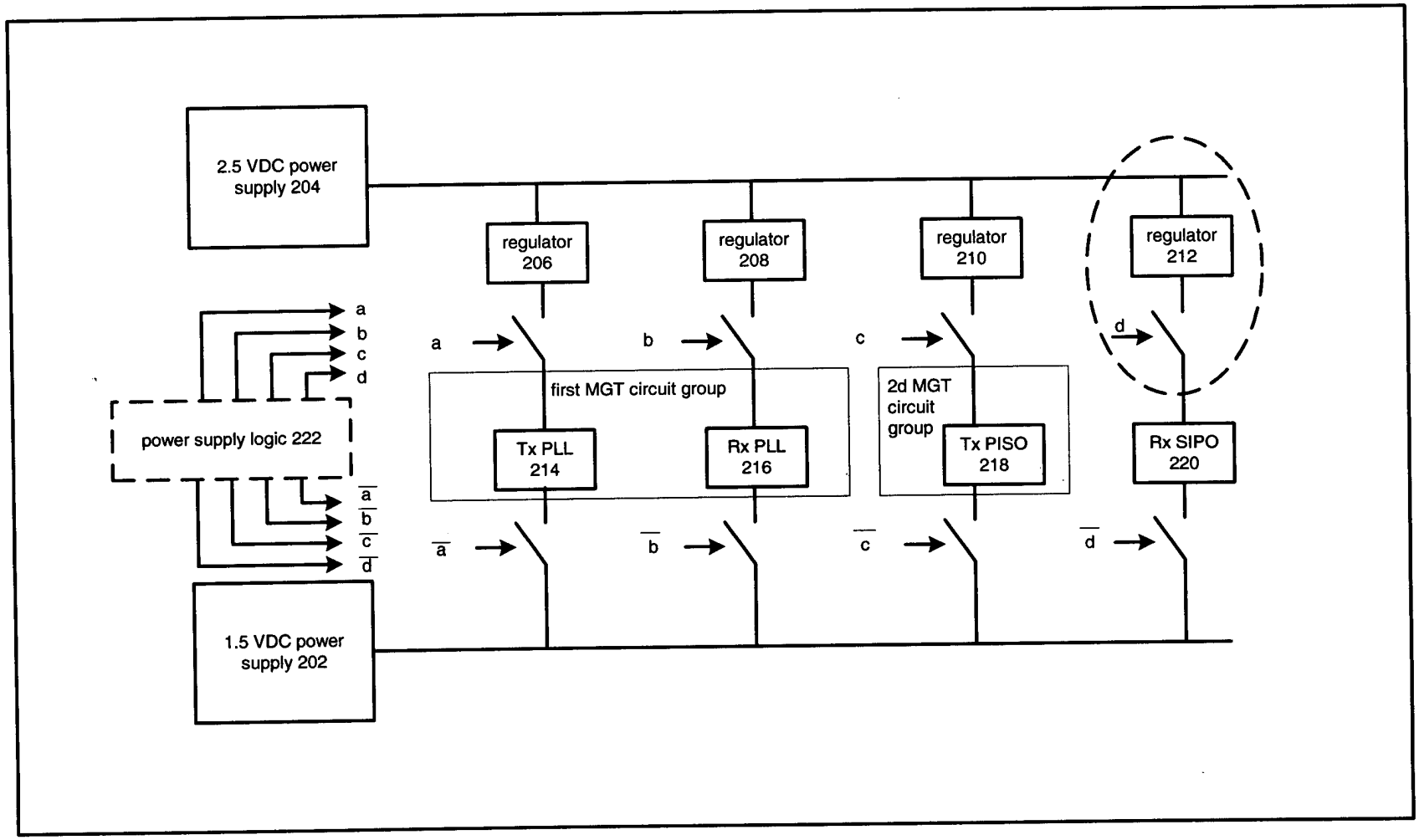

Figure 5
MGT FPGA 200

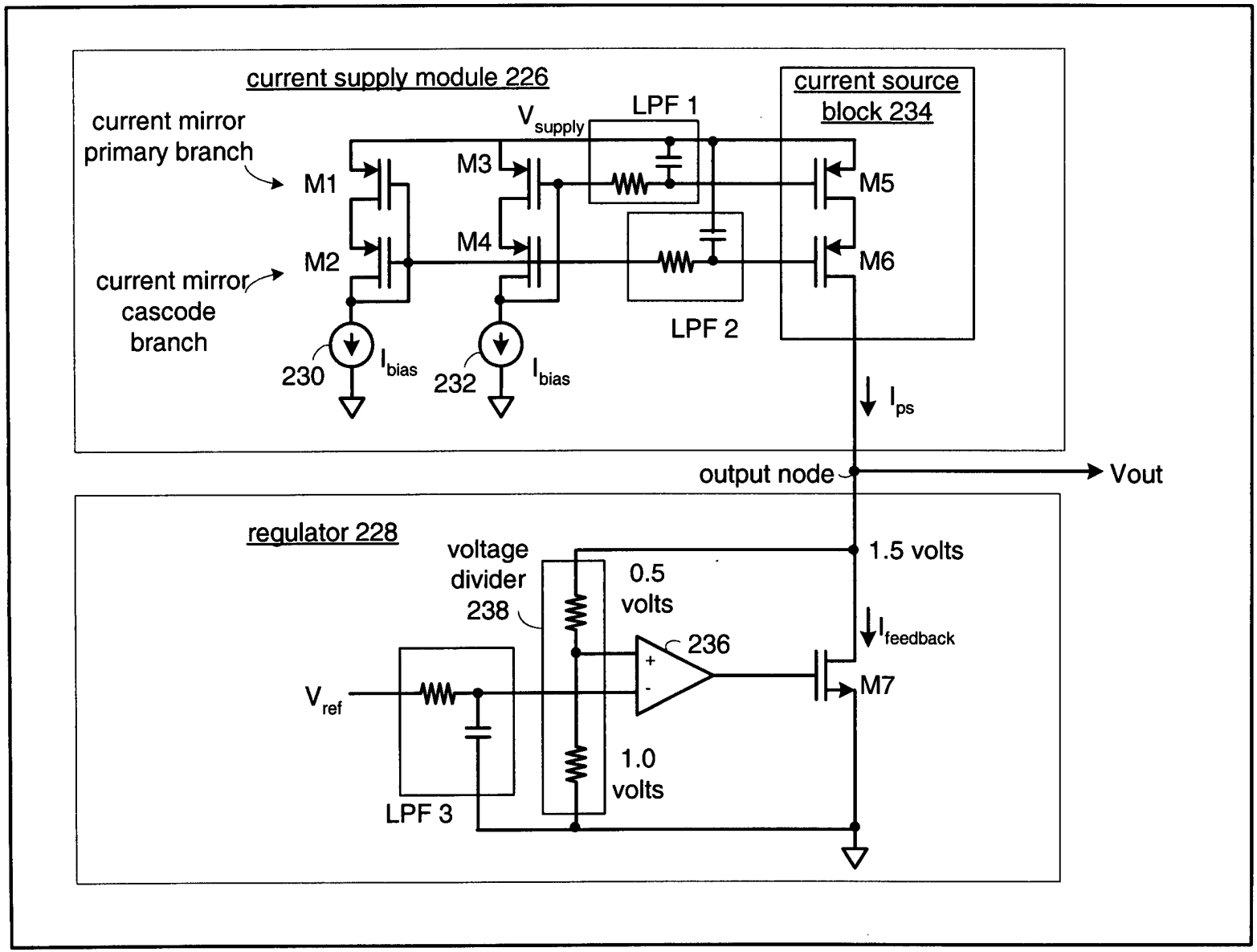

Figure 6
shunt regulator 224

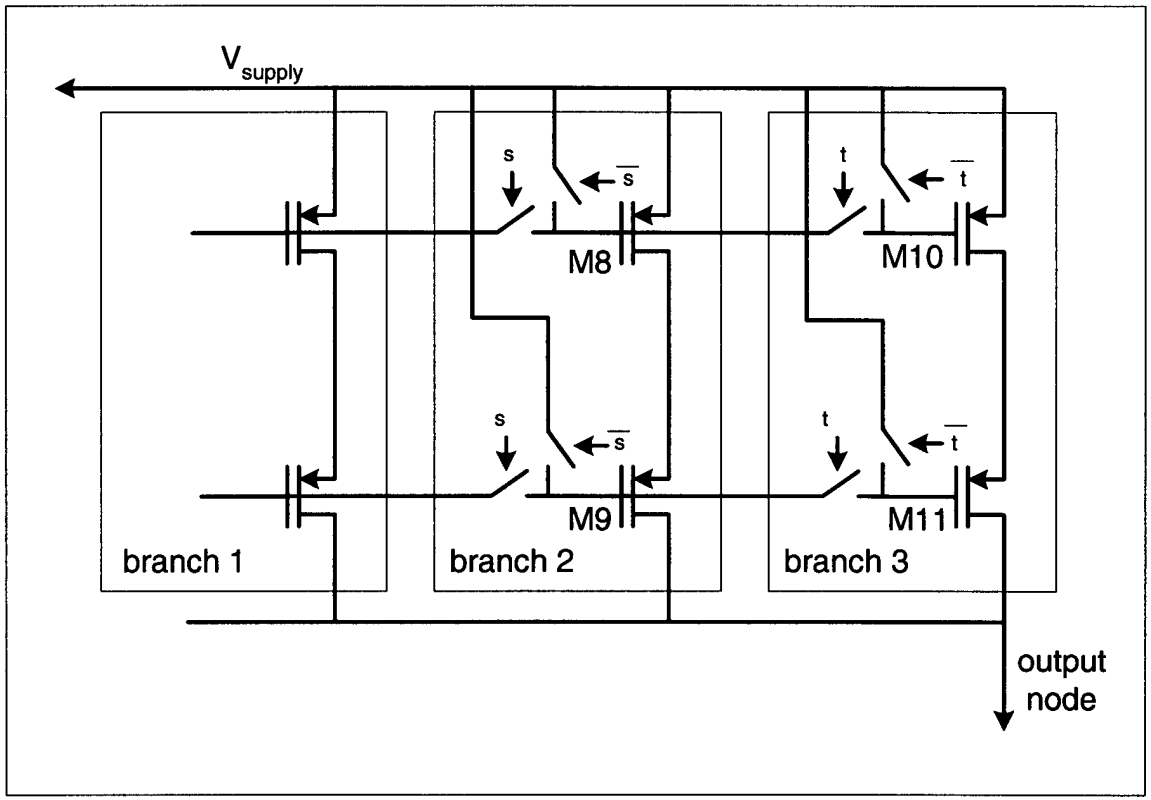

Figure 7

current source block 234

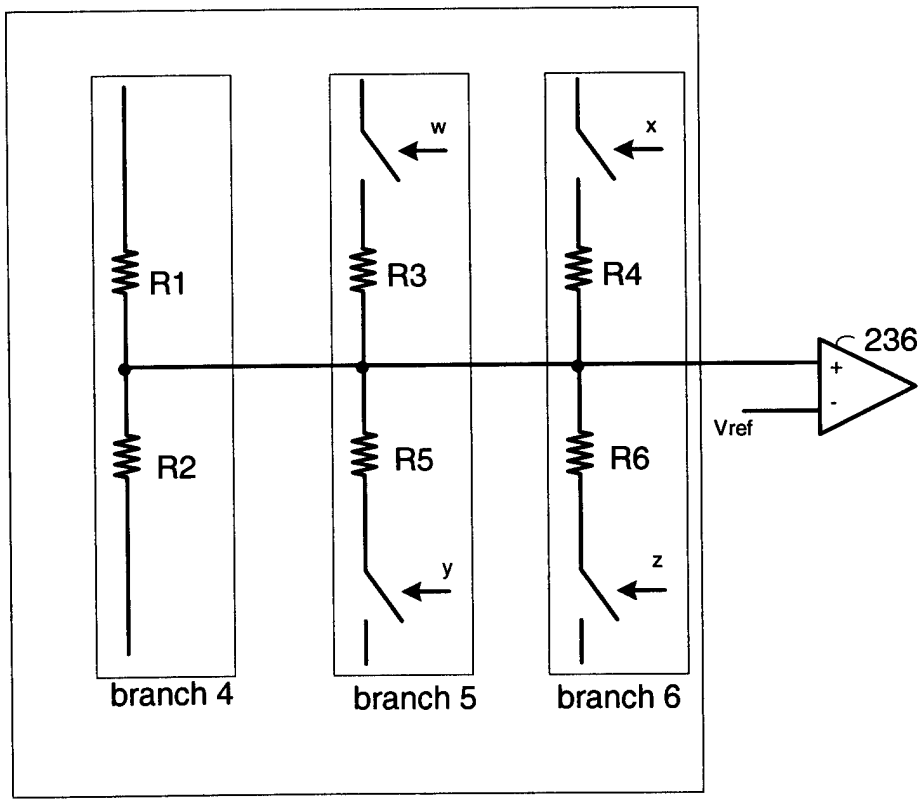

Figure 8

voltage divider 238

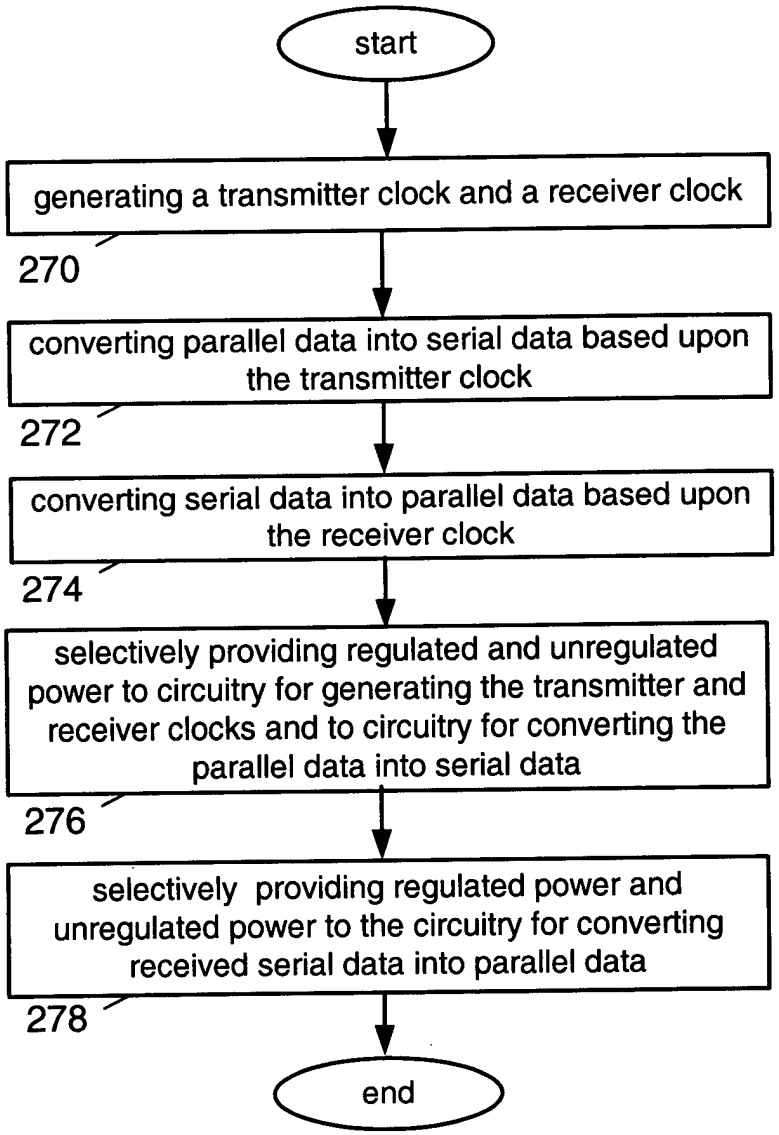

Figure 9

method for converting between parallel data and serial data

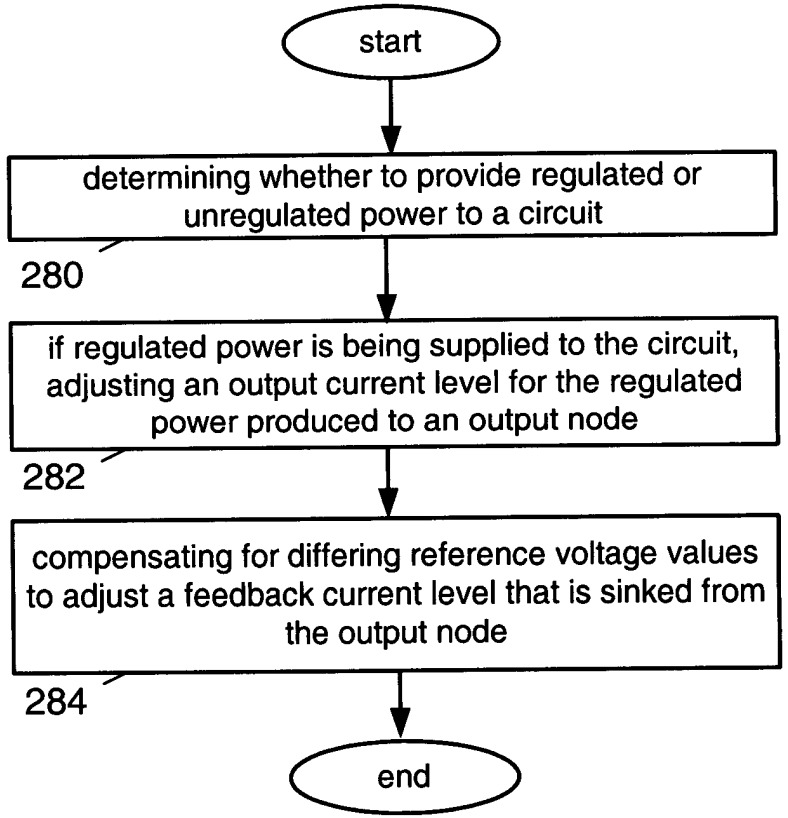

Figure 10

method for converting between parallel data and serial data